AMENDMENTS

In the Claims:

Please amend the claims according to the following listing of claims and substitute it for all prior versions and listings of claims in the application.

1. (currently amended) A chipset supporting multiple CPU's, comprising:

a first system logic circuit, applicable to the chipset and connected to a first type CPU;

a second system logic circuit, applicable to the chipset and connected to a second type CPU;

a double defined signal pin, used as a signal transmission pin;

~~an independent clock pin, coupled to the second system logic circuit as a clock signal pin, wherein the independent clock pin is isolated from other signal pins; and~~

a multiplex switch circuit, coupled to the first system logic circuit, the second system logic circuit and the double defined clock pin for establishing a first connection between the first system logic circuit and the double defined clock pin, and for establishing a second connection between the second system logic circuit and the double defined clock pin wherein the first type CPU may transfer signals with the first system logic circuit via the first connection and the second type CPU may transfer signals with the second system logic circuit via the second connection~~.~~; and

an independent clock pin, coupled to the second system logic circuit as a clock signal pin, wherein the independent clock pin forms an isolation path without coming across the multiplex circuit so as to be isolated from other signal pins.

2. (original) The chipset according to claim 1, wherein the first type CPU includes a Pentium series CPU and the second type CPU includes an AMD series CPU.

3. (original) The chipset according to claim 1, wherein a frequency transferred by the independent clock pin is higher than a frequency transferred by the double defined signal pin.

4. (original) The chipset according to claim 1, further comprising:

an independent strobe pin, coupled to the second system logic circuit as a strobe signal pin, wherein the independent strobe pin is isolated from other signal pins.

5. (original) The chipset according to claim 1, wherein a trace length between the independent clock pin and the second system logic circuit is shorter than a trace length of an address line or a control signal line of the chipset

6. (original) The chipset according to claim 1, wherein a space between the independent clock pin and other signal lines is larger than a space between two adjacent lines of address lines or between two adjacent lines of control signal lines of the chipset.

7. (original) The chipset according to claim 1, wherein the first connection is established when a control signal indicates the first type CPU is coupled with the chipset and the second

connection is established when a control signal indicates the second type CPU is coupled with the chipset.

8. (currently amended) A layout method of a chipset supporting multiple CPU's, wherein the chipset comprises a first system logic circuit used for coupling to a first type CPU and a second system logic circuit used for coupling to a second type CPU, the layout method comprising:

providing a double defined signal pin as a signal transmission pin;

providing a multiplex switch circuit;

coupling the multiplex switch circuit to the first system logic circuit, the second system logic circuit, and the double defined signal pin for establishing a first connection between the first system logic circuit and the first type CPU to transfer signals via the double defined signal pin, or for establishing a second connection between the second system logic circuit and the second type CPU to transfer signals via the double defined signal pin; and

providing an independent clock pin for coupling with the second system logic circuit for transferring signals, the independent clock pin forming an isolation path without coming across the multiplex circuit, wherein a frequency transferred by the independent signal pin is higher than a frequency transferred by the double defined signal pin.

9. (original) The layout method according to claim 8, wherein the first type CPU includes a Pentium series CPU and the second type CPU includes an AMD series CPU.

10. (original) The chipset according to claim 8, wherein a trace length between the independent clock pin and the second system logic circuit is shorter than a trace length of an address line or a control signal line of the chipset.

11. (original) The chipset according to claim 8, wherein a space between the independent clock pin and other signal lines is larger than a space between two adjacent lines of address lines or between two adjacent lines of control lines of the chipset.

12. (currently amended) A chipset supporting multiple central processing units, comprising:

a first system logic means for coupling to a first type CPU (central processing unit);

a second system logic means for coupling to a second type CPU;

a double defined signal pin for transferring signals;

~~an independent signal pin coupled to the second system logic means and isolated from other signal pins for transferring signals, wherein a frequency transferred by the independent signal pin is higher than a frequency transferred by the double defined signal pin; and~~

switch means, coupled to the first system logic means, the second system logic means and the double defined signal pin for establishing a first connection between the first system logic means and the double defined signal pin to transfer signals between said first system logic means and said first type CPU when a control signal indicates the first type CPU is coupled with the chipset, and for establishing a second connection between the second system logic means and the double defined signal pin to transfer signals between said second system logic means and said

second type CPU when the control signal indicates the second type CPU is coupled with the chipset~~.~~; and

an independent clock pin, coupled to the second system logic means for transferring signals, forming an isolation path without coming across the switch means, and isolated from other signal pins, wherein a frequency transferred by the independent clock pin is higher than a frequency transferred by the double defined signal pin.

13. (original) The chipset according to claim 12, wherein the first type CPU includes a Pentium series CPU and the second type CPU includes an AMD series CPU.

14. (original) The chipset according to claim 12, wherein said independent signal pin couples with a strobe pin or a clock pin of the second type CPU.

15. (original) The chipset according to claim 12, wherein a trace length between the independent clock pin and the second system logic circuit is shorter than a trace length of an address line or a control signal line of the chipset.

16. (original) The chipset according to claim 12, wherein a space between the independent clock pin and other signal lines is larger than a space between two adjacent lines of address lines or between two adjacent lines of control lines of the chipset.